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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LAMARRE, GUY J	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 10/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,579	HUMMEL, ULRICH HELMUT	
	Examiner	Art Unit	
	Guy J. Lamarre, P.E.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/302,139.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *17 March 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

0. Applicant's pre-amendment and IDS of *17 March 2004* have been entered. The Examiner has considered the IDS.

0.1 **Claims 1, 10, 18-19** and **21** are amended. **Claims 1-21** remain pending.

0.2 The rejections under 35 USC 112 of record are withdrawn in response to Applicants' amendment.

0.3 The prior art rejections of record to Claims **1-21** under 35 U.S.C. 103(a) as being unpatentable over **Applicants' Admitted prior art**, **Sher** (US Patent No. 5,973,900) and **Roohparvar** (US Patent No. 5,973,900) are withdrawn in response to Applicants' amendment.

Response to Arguments

1. Applicants' arguments of *17 March 2004* have been fully considered, and are deemed persuasive only to the extent that the approach, whereby 'supervoltage is applied to supply voltage terminal,' is not specifically disclosed by the prior art of record.

McClure (US Patent No. **5,493,532)** however discloses such supply voltage terminal arrangement, e.g., in col. 4 line 10 - col. 9 line 45 et seq., "***wherein said special test mode*** *corresponds* ***to a stress test; and further comprising: a power supply terminal, for*** *receiving* ***a power supply voltage near a first voltage in the normal operating mode, and for receiving a power supply voltage near a second, higher, voltage for the stress test.***"

Claim Rejections - 35 USC § 103

2. **Claims 1-21** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Applicants' Admitted prior art** (hereinafter **Admitted prior art**) in view of **Sher** (US Patent No. 5,973,900; October 31, 1997) in further view of **Roohparvar** (US Patent No. 5,973,900; DATE FILED: July 28, 1995) and **McClure** (US Patent No. 5,493,532).

As per Claims 1, 10, 18, 19, 21, Admitted prior art substantially discloses the claimed means for parametrization comprising: means to apply start command or start testing operation

or initiate circuit parametrization (page 1 line 8); means to circuit to indicate that parametrization process is activated (page 1 line 15); means to synchronize testing operation via e.g., oscillator, clock input and timing interfacing means (page 1 line 13); means to apply or transfer or store testing vectors or parameters during testing (page 1 line 13). {See **Admitted prior art,** page 1 line 7 – page 2 line 8, in passim, wherein apparatus and method are described.}

Not specifically described in detail in **Admitted prior art** is the step whereby potential or voltage levels exceeding normal operating voltage ranges are applied to exercise ICs. **However** overstressing circuitry in plural testing protocols is well known. For example, such protocols are implemented in burn-in or reliability tests. **Sher,** in an analogous art, discloses a '*High voltage protection for an integrated circuit input buffer,*' wherein such techniques are described {See **Sher,** Id., BACKGROUND OF THE INVENTION: para. 2.} **Therefore**, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure in the **Admitted prior art** by including therein potential exceeding means as taught by **Sher,** because such modification would provide the procedure disclosed in **Admitted prior art** with a technique whereby "*Testing includes "burn-in" where* ***the circuits*** *are* ***subjected to extremes*** *of operating temperatures and* ***voltages to identify infant failures***." {See **Sher,** Id., BACKGROUND OF THE INVENTION: para. 2.}

While Admitted prior art and **Sher** substantially disclose the procedure for the claimed invention, **they fail to specifically describe** that supervoltage is applied to two-or-plural pins or terminals in addition to the ground terminal.

However, such **supervoltage** application control technique is well known in memory systems, e.g., **Roohparvar,** in an analogous art, discloses a " *Memory system having non-volatile data storage structure for memory control parameters and method*," wherein such plural-pin

supervoltage application means is described. {See **Roohparvar,** Id., Fig. 14: *terminals 240 and 242*, and associated description in col. 22

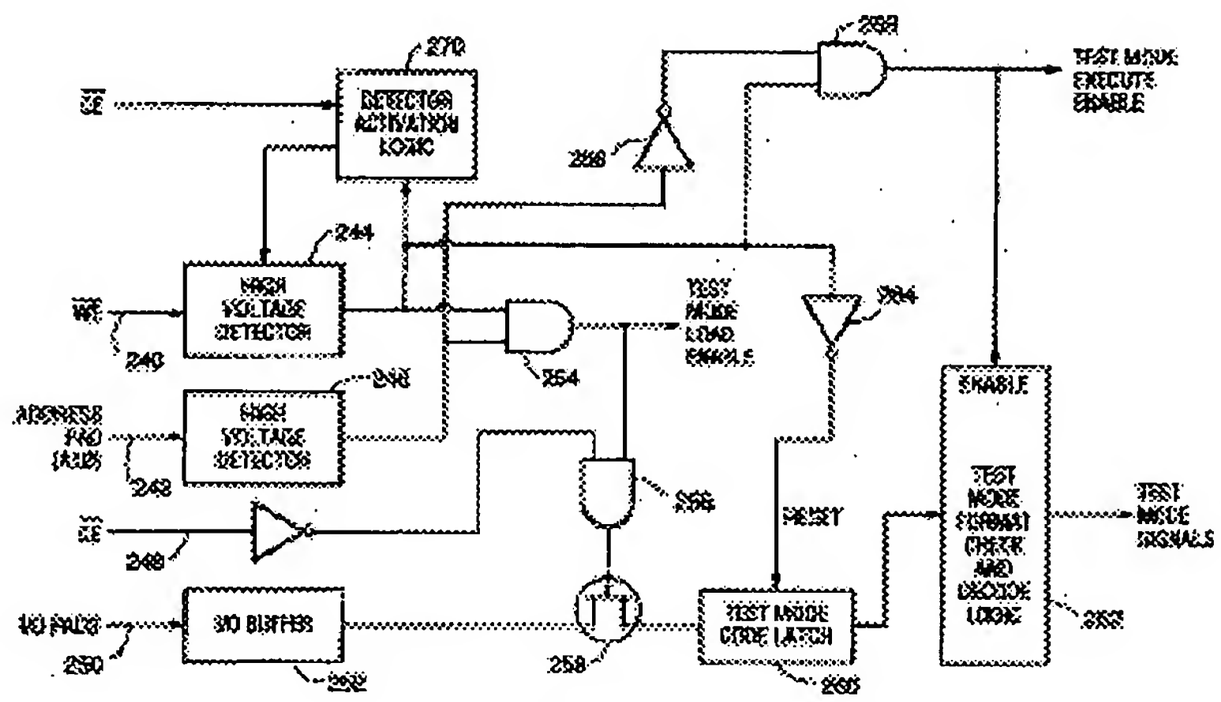

FIG. 14

and Abstract, in passim, e.g., "*Control circuitry is included for controlling memory operations, with the memory operations including programming the memory cells; reading the memory cells and preferably programming the cells. A plurality of non-volatile data storage units are provided for storing control parameter data used by the control means for controlling the memory operations. Such control parameters may can include, for example, parameters for adjusting the magnitude and duration of voltage pulses applied to the memory for carrying out programming and erasing operations.*"}

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of **Admitted prior art** and **Sher** by including therein *control means* as disclosed by **Roohparvar** because such modification would provide the procedure of **Admitted prior art** and **Sher** with " *a novel memory system having control parameters which may be adjusted after fabrication for optimum performance (col. 30 line 10)* " whereby "*FIG. 14 depicts one embodiment of a circuit for entering and executing test mode operations. Among other things, test mode commands must be applied to the data I/O terminals of the memory to indicate which one of various test modes is to be entered. Typically, the end user of the memory system would have no reason to cause the memory system to enter the test mode since*

this mode is intended to be used by the memory fabrication facility. Furthermore, accidental entry into the test mode is to be avoided since the memory could be rendered permanently inoperable in this mode. Thus, the test mode circuitry is designed to specifically reduce the likelihood of accidental entry into the test mode by requiring simultaneous application of high voltages to multiple memory system terminals. The FIG. 14 ***circuit is activated by application of a high voltage to two or more terminals 240 and 242 of the memory system from an external source****.*

These terminals are non-dedicated terminals used during normal memory operations. Terminals 240 and 242 may include, for example, address terminal (pad) A10 and the write enable terminal WE. The magnitude of the high voltage applied to terminals 240 and 242 is chosen to be outside of the range of voltages, which would typically be applied to those terminals during use of the terminals in normal (non-test mode) operation of the memory system. This is done to prevent an end user from unintentionally entering the test mode. The high voltage applied to terminals 240 and 242 is detected by detectors 244 and 246. ... After application of the high voltage to terminals 240 and 242, a signal on another terminal 248, in this case the chip enable CE terminal, is made active (low). Test code data corresponding to one of several possible test modes is placed on the data I/O terminals 250 of the memory and forwarded to an I/O buffer 252." {See **Roohparvar,** Id., col. 22 line 12 et seq.}

While Admitted prior art/Sher/Roohparvar substantially disclose the procedure for the claimed invention, **they fail to specifically describe** that supervoltage is applied to the supply voltage pins or terminals.

However, as suggested as follows below, such **supervoltage** application control technique is well known in memory systems, e.g., **Roohparvar** does not restrict supervoltage application exclusively to address/write enable pins: non-dedicated terminals may also be supply voltage pins/terminals in Fig. 14: *terminals 240 and 242*, and associated description in col. 22 et seq.

Accordingly, McClure, in an analogous art, sketches/lays out such a supply voltage terminal arrangement, e.g., in Fig. 1 and col. 4 line 10 - col. 9 line 45 et seq., "*wherein said special test mode corresponds to a stress test; and further comprising: a power supply terminal, for receiving a power supply voltage near a first voltage in the normal operating mode, and for receiving a power supply voltage near a second, higher, voltage for the stress test.*"

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of **Admitted prior art/Sher/Roohparvar** by including therein supply voltage terminal arrangement as disclosed by **McClure** because such modification would provide the procedure of **Admitted prior art/Sher/Roohparvar** with a cost/hardware savings technique whereby allocation of a terminal/pin/pad exclusively dedicated for supervoltage application is avoided. {See McClure, Id., Fig. 1 and col. 9 line 45 et seq.}

As per Claim 2, Admitted prior art teaches the procedure for the claimed means for parametrization including means wherein a first logic state of a bit by an additional edge change .... {See **Admitted prior art,** Id., page 1 line 13, wherein means is provided for clock signal adjustment via oscillator.}

As per Claim 3, Sher teaches the procedure for the claimed means for parametrization including code with plural bits, and wherein after each bit includes an edge thereof is changed, or means to change clock signal. {See **Sher,** Id., SUMMARY OF THE INVENTION: para. 2, wherein means is provided for monitor test results, to assign states, and synchronize testing, e.g., "*To **ensure the state** of the output of the buffer circuit while the n-channel transistors are thus isolated or floating, the n-channel transistors connected to receive an input signal to be buffered are clamped to the supply voltage. A p-channel transistor is connected between the drain of the first n-channel transistor in the series chain of transistors and the supply voltage to provide the supply voltage clamp in response to the control signal.*"}

As per Claim 4, Admitted prior art teaches the procedure for the claimed means for parametrization means wherein IC includes oscillator and interface device for processing clock... {See **Admitted prior art,** Id., page 1 line 13, wherein means is provided for clock signal adjustment via oscillator, and means to transfer data into device under test.}, and Sher teaches means to set up timing windows to effect and monitor testing. {See **Sher,** Id., SUMMARY OF THE INVENTION: para. 2, wherein means is provided for monitoring test results, to assign states, and synchronize testing, e.g., "*To **ensure the state** of the output of the buffer circuit while the n-channel transistors are thus isolated or floating, the n-channel transistors connected to receive an input signal to be buffered are clamped to the supply voltage. A p-channel transistor is connected between the drain of the first n-channel transistor in the series chain of transistors and the supply voltage to provide the supply voltage clamp in response to the control signal.*"}

As per Claim 5, Sher teaches the procedure for the claimed means for parametrization means wherein time duration of the bit is determined following the occurrence of least one edge... {See **Sher,** Id., Fig. 1 and DETAILED DESCRIPTION OF THE INVENTION: para. 5, wherein means is provided for monitoring test results, to assign states, and synchronize testing, e.g., "*An alternate or second embodiment of the present invention is illustrated by the dotted line structure of FIG. 1. In particular for this embodiment, a p-channel clamp transistor 142 is coupled between the drain D of the first n-channel transistor 114 and the supply voltage VCC. The gate electrode of the clamp transistor 142 is coupled to the input pad 140 to receive the control signal and clamp the drain D of the first n-channel transistor 114 to the supply voltage VCC. This embodiment protects the n-channel transistors of the input inverter 102 against high voltage applied to the gate electrode of the first n-channel transistor 114 and also ensures **the output state** of the buffered output signal from the input buffer 100 **during the time** that a high voltage is applied to the input pad 106. Since the source S and drain D electrodes of the*

transistor 114 and the drain D electrode of the n-channel transistor 116 ***are no longer floating*** *but clamped to VCC, some high voltage protection is* ***forfeited to ensure the output state*** *of the input buffer 100.* "}

As per Claim 6, Sher teaches the procedure for the claimed means for parametrization means wherein time duration of the bit is determined from average of least two consecutive bits. {See **Sher,** Id., Fig. 1 and DETAILED DESCRIPTION OF THE INVENTION: para. 5, wherein means is provided for monitoring test results, to assign states, and synchronize testing, e.g., "*An alternate or second embodiment of the present invention is illustrated by the dotted line structure of FIG. 1. In particular for this embodiment, a p-channel clamp transistor 142 is coupled between the drain D of the first n-channel transistor 114 and the supply voltage VCC. The gate electrode of the clamp transistor 142 is coupled to the input pad 140 to receive the control signal and clamp the drain D of the first n-channel transistor 114 to the supply voltage VCC. This embodiment protects the n-channel transistors of the input inverter 102 against high voltage applied to the ... of the first n-channel transistor 114 and also ensures* ***the output state*** *of the buffered output signal from the input buffer 100* ***during the time*** *that a high voltage is applied to the input pad 106. Since the source S and drain D electrodes of the transistor 114 and the drain D electrode of the n-channel transistor 116* ***are no longer floating*** *but clamped to VCC, some high voltage protection is* ***forfeited to ensure the output state*** *of the input buffer 100.* "}

As per Claims 7, 11, 13, 15, Sher teaches the procedure for the claimed means for parametrization means for storing specification adjustments and means to activate circuitry adjustment. {See **Sher,** Id., BACKGROUND OF THE INVENTION: paras. 2-3, for means to store test vectors or spec data, activate such test, and adjust circuitry, e.g., "*Integrated circuits are tested to ensure that they are free of defects and that the circuits function properly and* ***according to specifications****. Testing includes "burn-in" where the circuits are subjected to extremes of operating*

temperatures and voltages to identify infant failures. Alternate testing can be performed on integrated circuits to ***test application specific features****. Since alternate testing is normally performed by the manufacturer and is not intended to be used by purchasers of the integrated circuits, an electronic key is typically provided to enable the manufacturer to place the circuits into a test mode. A common key is a voltage which is a predetermined level above the maximum specified supply voltage for the circuits. Thus a high voltage key, sometimes referred to as a "supervoltage", may be applied to an input pin of an integrated circuit to place the circuit in a test mode. Once in the test mode, test vectors can be entered using other pins of the integrated circuit to perform required tests. In some integrated circuits, defects can be corrected by means of one time programmable (OTP) permanent electrical connections which can be implemented with an antifuse. In dynamic random access* ***memories (DRAMs)****, failing memory cells, rows or columns which are detected during testing can be remapped to functional redundant memory cells, rows or columns by selective permanent programming of antifuse elements. OTP connections are also used to* ***permanently store data*** *on integrated circuits such as programmable logic arrays* ***(PALs),*** *programmable logic devices and programmable read only memories* ***(PROMs)*** *and for other integrated circuit applications. An antifuse element is programmed by* ***applying a programming voltage ranging from approximately 9 volts to approximately 13 volts which is above the maximum supply voltage for the integrated circuits.*** *"}*

As per Claims 8, 12, 14, 20, Sher teaches the procedure for the claimed means for parametrization means for confirming parametrization process and detection setting feature. {See **Sher,** Id., BACKGROUND OF THE INVENTION: paras. 2-3, for means to set or confirm parametrization process via a pin or terminal or a key or sensor, e.g., "*Since alternate testing is normally performed by the manufacturer and is not intended to be used by purchasers of the integrated circuits, an* ***electronic key*** *is typically provided to enable the manufacturer to place the circuits into a test mode. A common key is a voltage which is a predetermined level above the maximum specified supply voltage for the circuits. Thus a high voltage key, sometimes referred to as a "supervoltage", may be*

applied to an input pin of an integrated circuit to place the circuit in a test mode. Once in the test mode, test vectors can be entered using other pins of the integrated circuit to perform required tests. In some integrated circuits, defects can be corrected by means of one time programmable (OTP) permanent electrical connections which can be implemented with an antifuse. In dynamic random access memories (DRAMs), failing memory cells, rows or columns which are detected during testing can be remapped to functional redundant memory cells, rows or columns by selective permanent programming of antifuse elements. OTP connections are also used to permanently store data on integrated circuits such as programmable logic arrays (PALs), programmable logic devices and programmable read only memories (PROMs) and for other integrated circuit applications. An antifuse element is programmed by applying a programming voltage ***ranging from approximately 9 volts to approximately 13 volts which is above the maximum supply voltage for the integrated circuits.*** *"*}

As per Claims 9, 15-16, Sher teaches the procedure for the claimed means for parametrization means for identifying the integrated circuit. {See **Sher,** Id., BACKGROUND OF THE INVENTION: paras. 2-3, for means to set or confirm parametrization process, including identifying, detecting based on sync bit, address bit, data bit, instruction or command bit and re-mapping means, e.g., " *In dynamic random access memories (DRAMs),* ***failing memory cells, rows or columns*** *which are* ***detected*** *during testing can be* ***remapped*** *to functional redundant memory cells, rows or columns by selective permanent programming of antifuse elements. OTP connections are also used to permanently store data on integrated circuits such as programmable logic arrays (PALs), programmable logic devices and programmable read only memories (PROMs) and for other integrated circuit applications. An antifuse element is programmed by applying a programming voltage ranging from approximately 9 volts to approximately 13* ***volts which is above the maximum supply voltage for the integrated circuits.*** *"*}

As per Claim 17, Sher teaches the procedure for the claimed means for parametrization means for sensor by Hall sensor or means to detect circuit status. {See **Sher,** Id., BACKGROUND OF THE INVENTION: paras. 2-3, for means to set or confirm parametrization

process, including identifying, detecting based on sync bit, address bit, data bit, instruction or command bit and re-mapping means, e.g., ". *In dynamic random access memories (DRAMs),* ***failing memory cells, rows or columns*** *which are* ***detected*** *during testing can be* ***remapped*** *to functional redundant memory cells, rows or columns by selective permanent programming of antifuse elements."}

As per Claim 20, Roohparvar teaches the procedure for the claimed means for parametrization means wherein number of pins stays the same during parametrization process. {See **Roohparvar,** Id., col. 22 line 12 et seq., e.g., "*The FIG. 14* ***circuit is activated by application of a high voltage to two or more terminals 240 and 242 of the memory system from an external source****. These terminals are non-dedicated terminals used during normal memory operations. Terminals 240 and 242 may include, for example, address terminal (pad) A10 and the write enable terminal WE."*}

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

3.1 Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (703) 872-9306 for all formal communications.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Fourth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (703) 305-0755. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached at (703) 305-9595.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Guy J. Lamarre, P.E
Primary Examiner
10/22/04